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Innovative Defense Techniques for damping Digital to RF Crosstalk

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Abstract

"Everyone going Mobile" is the current communication trend. Mobile devices such as Smartphones and Tablets are becoming increasingly popular in uploading movies and pictures to Facebook and YouTube. The communication is carried out by antennas operating in many bands such as the GSM band at 900 MHz or BT at 2.4 GHz. Data storage for the communication process is provided by a memory bus DDR2/3 operating at 1066MTs and IO communication is provided by a USB3.0 type bus operating at 2.5GHz. These critical interfaces couple noise to the transmitting/receiving antennas which can corrupt the voice/data wireless communication link. This paper proposes studies of the main physical mechanisms behind such noise coupling to the antennas. We used a massively parallel finite difference time domain (FDTD) EM solver to find the optimum phase shift between the byte lanes resulting in a 50% reduction of crosstalk between memory and the multiband antenna. We developed an innovative process/workflow using EDA tools and measurements to solve such problems.

Author(s) Biography

Davy Pissoort was born in 1978. He received the M.S. and Ph.D. degrees in electrical engineering from Ghent University, Ghent, Belgium, in 2001 and 2005, respectively. From October 2005 to October 2006, he was a Postdoctoral Researcher with the Fund for Scientific Research-Flanders (Belgium) (FWO-Vlaanderen) at the Department of Information Technology, Ghent University. In November 2006, he joined the Eesof-EDA Department, Agilent Technologies, Ghent, Belgium, as a Research Engineer. Since August 2009, he is with the KU Leuven, Campus Ostend, Belgium where he is also head of the Flanders' Mechatronics Engineering Centre. His current research interests include the development of fast and efficient electromagnetic simulation methods, electromagnetic compatibility, as well as the analysis and testing of the mechanical and thermal reliability of electronic modules.

Hany Fahmy is WW-Business-Development & Master Application Expert for HSD at Agilent Technologies. Before joining Agilent, Hany was the director of SIE/EMC System Design and Manufacturing at NVIDIA, dealing with the design and analysis of high-speed digital and analog interconnecting systems (DDR3, GDDR3/5, LVDS, HDMI/DP & PCIe) for GPU boards and the Tegra Smartphone systems. Before joining NVIDIA, he worked at Intel for 10-years heading the Memory Architecture Group (MAG) designing system memory (PC100/133, Rambus & DDR1/2/3) for desktop, notebook and workstations based on Intel chipsets and microprocessors. Hany also worked at Micron and TI. He has a Ph.D. in Computational Electromagnetics of MMIC from the University of Toronto and an M.Sc. and a B.Sc. from Cairo University in Egypt.

Mehdi Mechaik is currently with NVIDIA Corp working as a senior signal integrity engineer focusing on RF and PCB analysis and design. He has a PhD and a Masters of Science degree from the University of Arizona in electrical and computer engineering where he also did research on computational electromagnetics. Prior to that Dr. Mechaik worked for Advanced Micro Devices from 2001 to 2008 as a member of technical staff in processor package and board designs. From 1997-2001 he worked for Cisco Systems as a software engineer working on cable and modem designs. He also taught electrical engineering courses as an adjunct professor at the Northern Arizona University in the period 1995-1997 and did a post-doctoral research at the University of Arizona in 1994-1995.

Henry Zeng was born in 1981. He received the Bachelor and Master degrees in Mechanical and Electronic Engineering from Xidian University, Xi'an, China, in 2007. From March 2004 to March 2007, he attended a research funded by Chinese government, which studied the coupling among forces/stress/ vibration, heat and electromagnetic field in electronic devices. He was mainly responsible for the electromagnetic field. In April 2007, he joined NVIDIA. He is focusing on EMC/RF design, analysis and certification and antenna design and analysis

Charlie Shu
is currently an Engineering Manager at NVIDIA Crop. He joined NVIDIA as a senior engineer in 2001. Previously, he had held engineer, technical staff, and senior technical staff positions in several Silicon Valley companies, including Apple Inc. and Sun Microsystems since 1987. He holds a BSEE degree from Beijing University of Technology and a MSCS degree from Ohio University.

Charles Jackson is an SI/EMC Compliance Engineering Manager at NVIDIA Corporation. He has over 30 years' experience in the EMC field working in the areas of medical devices, commercial/military avionics, consumer electronics, and passive components. He received his BSEE from the University of Minnesota.

Jan Van Hese received his engineering degree in Electronics (specialty High-Frequency Modeling) from the University of Gent, Belgium in 1988 and a PhD. degree from the same University on EM modeling and simulation in 1993. After finishing his PhD in 1993, he started working for the Alphabit company located in Gent, Belgium as a software developer. This company was a spin-off of from Imec working on the development of the planar EM simulator Momentum which was commercialized by Hewlett-Packard. In 1994 the Alphabit company was acquired by Hewlett-Packard. In terms of development work, Jan Van Hese contributed to the Green function module and the farfield calculation module within the Momentum product. In 1998, he became an R&D project manager responsible for the Momentum product as a whole within the EEsof division. In 1999 EEsof became part of Agilent Technologies after the creation of the Agilent spin-off from HP. Currently Jan Van Hese is responsible for the development the 3D EM products within Agilent EEsof,. Jan Van Hese is author of one patent

application and multiple technical papers in the field of EM modelling and simulation techniques.

1. Introduction

Due to the increasing overall complexity and integration, Electro-Magnetic Interference (EMI) issues on printed circuit boards (PCBs) are nowadays highly complex system level problems because of many aspects [1], such as: skew, rise-fall mismatch, delays, reflections, crosstalk, delta-I noise, un-intentional and intentional antenna radiation, and other effects. Mobile devices such as smartphones, tablets, portable PCs and others have multiple-input-multiple-output (MIMO) on-board antennas. Designing and implementing such on-board antennas leads to two major challenges, making it crucial to co-design the printed circuit board with the on-board antennas.

It is the purpose of this paper to show an analysis of the main noise sources and how to reduce the noise by a significant amount thereby making the communication link more immune to interference problems.

1.1 Design challenges related to on-board antennas

The first challenge is that these antennas have to be small, while still maintaining the required performance. Typical frequencies for which antennas have to be designed are 900 MHz and 1800 MHz (GSM), 1.57 GHz (GPS), 2.4 GHz (Bluetooth, WLAN), and 5 GHz (WLAN). Due to their small physical size, the on-board antennas rely on the existence of a large ground plane on the PCB to aid in their performance [2]. As will be shown in this paper, changing the ground-plane shape (width, height, slots, holes, stitching vias,…) can have a big influence on both the resonance frequencies and the resonance depths. Similarly, changing the antenna location along the ground plane can have a significant impact as well. Antenna currents are induced in a large part of the PCB ground planes and can even reach regions that are physically far away from the antenna location.

The second challenge is that the PCBs contain a lot of high speed digital interfaces such as DDR2/3 or IO buses like USB3.0 or HDMI which can easily interfere with other parts on the PCB, certainly including the on-board antennas and their attached circuitry. When looking into more detail at the interference between digital and on-board antennas, one can conclude that the interference actually happens in two-ways, depending on whether the antenna is in receive or in transmit mode:

- If the antenna is in receive mode, it will have to be able to successfully receive and process very small signals. As the induced useful voltages at the antenna ports are typically very small, any noise that is induced at those ports leads to a significant decrease of the sensitivity of the receiver circuit. Hence, in receive mode, care has to be taken that the EMI coupling from the on-board digital circuits to the on-board antennas is kept small. Note that in some parts of the world (e.g. Europe [3]), there are even legal requirements that state that the total isotropic sensitivity of the receiving circuit should be above a given limit, before the mobile device can be put onto the market.

- If the antenna is in transmit mode, it will have to send out a significant amount of power (e.g. 2 Watt for GSM). This means that there are high voltages and currents at the antenna ports which can couple significantly to the digital interfaces thereby increasing bit error rates.

One of the first rules to avoid interference on PCB level is to partition the PCB in an intelligent way, such that critical noise sources (e.g. high-speed digital circuits, memories,…) are placed far away from sensitive parts (e.g. analog receivers) [4]. The EMI reduction due to partitioning relies mainly on the physical phenomenon that above a few MHz return currents tend to stay very close to their signal current path in order to reduce the overall inductance of the total current path. So as long as this return current path is not disturbed (e.g. by use of full ground-planes), all currents will be very "local" on the specified part of the PCB and will not interfere heavily with circuits at other places on the PCB. As explained above, when there are on-board antennas these will induce antenna currents in large parts of the ground planes on in PCB and even in regions that are far away from the physical location of the antenna. Hence, when partitioning the PCB, one has to know the distribution of these antenna currents in order to reduce the EMI to and from these antennas.

In this paper it will be shown that indeed the coupling through the interaction between the antenna currents induced in the ground planes and the return currents of digital traces is the major contributor for the EMI between digital and antenna currents. As a consequence, simple passive measures at which one would think immediately to reduce the EMI (e.g. on-board shielding) don't give much improvement. The most important aspect is to know how the antenna currents are distributed in the ground-plane, to put the digital in a region where these currents are small for the critical frequencies, and to make sure that there are no return path discontinuities of the digital current loops.

1.2 Virtual antenna/EMI lab

Unfortunately, many first prototypes fail to pass all specified design-requirements (multi-band operation, gain, battery life, mismatch, PA circuits,…) and certification tests (e.g. SAR, HAC, EMI,…), causing a big loss of time and profit. The main reason is that up to now for debugging these antenna and EMI issues one has to mainly rely on measurements done in costly anechoic chambers (5m and 10m chambers) or with EM near-field probes, scanners,... All these measurements require the existence of a first physical prototype and lab hardware resources. As a result, these tests are done rather late in the design cycle when there is not much flexibility left to implement the optimal and most cost-efficient mitigation methods. Moreover, these physical measurements don't always give sufficient debugging information over the possible cause of or solutions for the issues under study as they don't allow "to look into the PCB itself".

It is clear that it is of crucial importance to be able, very early in the design process (i.e. even before actually making a physical prototype), to (i) find the root cause of possible issues and (ii) check if all required specifications are fulfilled. Simulations offer a lot of flexibility when estimating the impact of different elements in the complete antenna

system and can really help to find the real sources for possible issues from the start of the design cycle. A big advantage of simulations is that they allow looking for quantities which are impossible or at least very hard to measure. With simulations, it is e.g. straightforward to obtain the current densities on the PCB ground planes either in time or frequency domains. This offers the design engineer an increased physical insight which leads to more efficient cost-competitive solutions.

Besides of the theoretical background of and the mitigation methods for the coupling between digital and on-board antennas, this paper also gives an overview of some efficient methodologies that are currently used by EMI engineers and designers within Nvidia Corporation to design performance and cost-effective EMI suppression techniques by means of a virtual antenna/EMI lab and this both early in the design process (pre tape-out) or after physically testing a first prototype (post tape-out) (Fig. 1).

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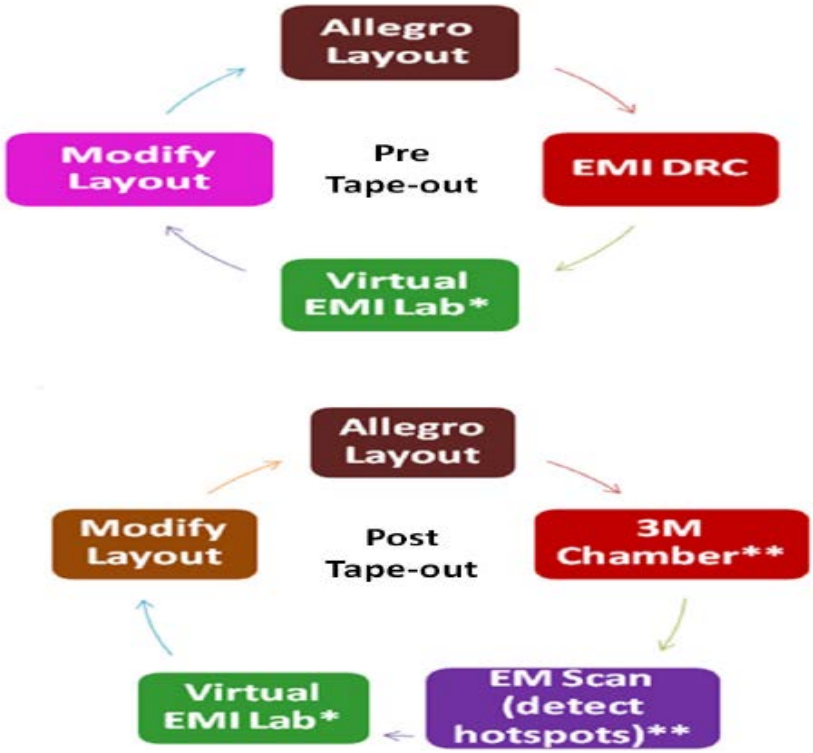


Figure 1: Pre-layout (top) and post-layout (bottom) virtual EMI lab process flows

1.3 GPU acceleration of full-wave EM simulations

Up to now, reliably and efficiently simulating the behavior of a complex multi-band mobile phone antenna together with a printed circuit board, a matching circuit, and an antenna housing has been a very hard task to accomplish. Due to the high geometrical complexity, the bottleneck most often has been the available computational power. However, thanks to the combination of the progress made by commercial electromagnetic

simulation tools and the recent advances in heterogeneous-computing: CPU parallel processing and GPU acceleration of those EM simulation tools, it becomes feasible to get accurate predictive simulation results of very complex designs in a reasonable amount of time. This opens the possibility to simulate the electromagnetic waves emitted from very detailed models of personal wireless communication devices, to accurately estimate the expected battery life, to evaluate the SAR in standardized head and body models, to study the detuning of the antenna characteristics when the mobile device is close to a human body, and to determine real world effects on system performance.

In this paper, all full-wave simulations are done with the CUDA enabled Finite-Difference Time-Domain (FDTD) solver that is included in Agilent Technologies' 3D EM platform EMPro [5]. When taking advantage of GPU acceleration, structures with this level of complexity can be successfully studied in reasonable amount of time (e.g., less than a day), while previously this would have taken up a week or even more to do. The full-wave FDTD method [6] is very suitable for characterizing complex boards for wideband applications. As a time-domain solver it has the advantage that it can capture both broadband (e.g. S-parameters) and steady-state results (e.g. far-fields) in one single simulation run. Thanks to its relative simple meshing, it offers a lot of flexibility to efficiently handle very complex 3D structures. Finally, due to their inherent parallel nature, the FDTD update equations are extremely well suited for GPU acceleration. Nvidia's GPUs are based on the massively parallel general purpose processor architecture called CUDA [7]. Nowadays, CUDA-based GPUs are being used in a variety of applications ranging from oil and gas exploration, financial computing, medical imaging, MATLAB simulations, and space explorations.

1.4 Overview of the paper

The remaining part of this paper is organized as follows. Section 2 describes the interaction between PCB ground planes (GP) and on-board antennas. It is shown how changing the GP shape or the location of the antenna along the ground plane changes the antenna characteristics. Further, some typical distributions of the induced antenna currents in the ground plane are also shown. In Section 3, it is proven that the interaction between the antenna currents induced in the ground plane and the return currents of (digital) signals is the major contributor to the coupling between digital traces and on-board antennas. In Section 4, a novel technique for mitigating such noise coupling from the digital traces to the antenna is described. By means of the virtual antenna/EMI lab, the optimum phase shift between memory bus byte lanes is investigated resulting in a 50% reduction of crosstalk between the digital memory and the antenna. Finally, Section 5 gives some concluding remarks.

2. Interaction between a ground plane and on-board antennas

2.1 Antenna description

The antenna used as an example in this paper is a folded, multiband planar monopole antenna whose design is inspired by the antenna described in [8]. The design requirements are that the antenna should have good performance around 900 MHz and from 1.7 GHz up to 2.5 GHz. Moreover, it should fit within a volume of 20.0 mm by 8.0 mm by 4.0 mm. The volume restriction on the antenna is a result of accommodating cellular or tablet form factors and is not a limitation on the techniques presented in this paper. The antenna geometry is shown in Fig. 2. The permittivity of the blue material supporting the antenna metallizations is 2.2.

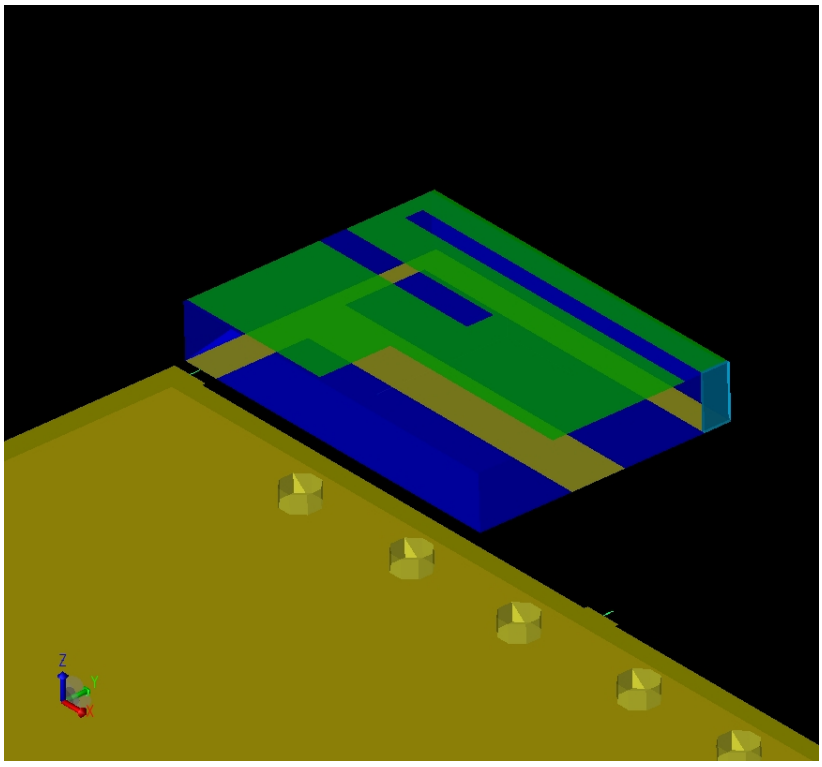


Figure 2: Antenna under study

2.2 Influence of the GP shape on the antenna performance

In this section, the influence of the ground-plane shape on the antenna characteristics is investigated. First, a rectangular ground-plane is considered whose length and width is changed (Fig.3). The antenna is always mounted on the top left side of the ground-plane. Figure 4 shows the antenna insertion loss when the length of the ground-plane is varied

from 6 cm to 11.5 cm, while the width of the ground-plane is kept constant at 5 cm. Figure 5 shows the antenna insertion loss when the length of the ground-plane is kept constant at 8 cm, while the width of the ground-plane is varied from 4.5 cm to 6 cm.

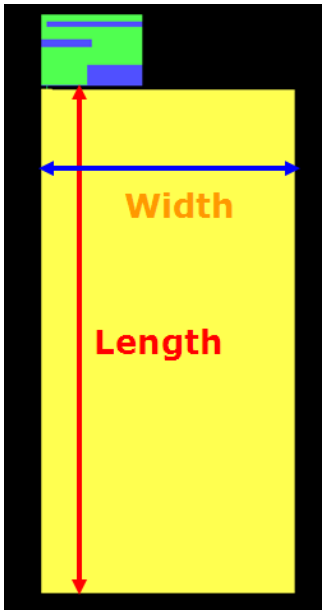


Figure 3: Antenna mounted on a rectangular ground-plane

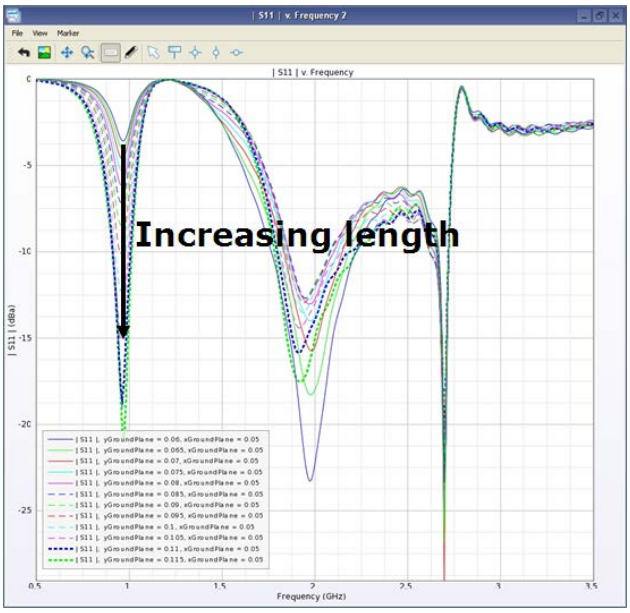


Figure 4: Influence of variable GP length (width fixed).

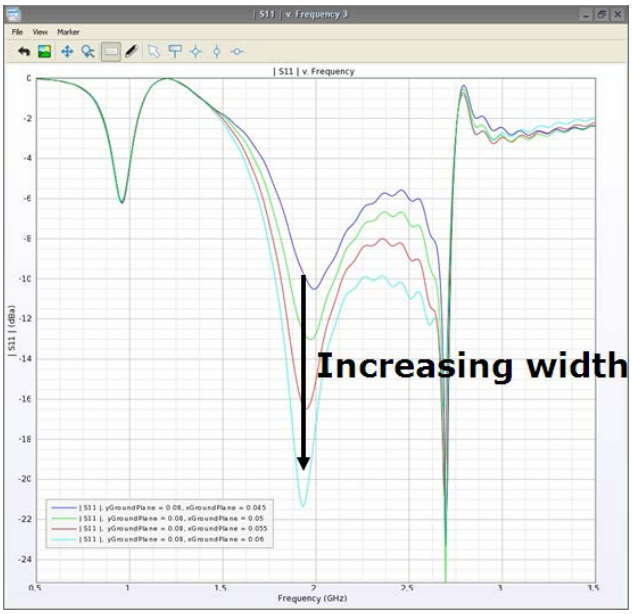


Figure 5: Influence of variable GP width (length fixed)

It is seen that the length and width have a difference influence of the antenna performance. Increasing the GP length mainly influences the depth of the first resonance at 900 MHz, where a longer ground-plane equals a better matched antenna. Increasing the width of the GP has no influence on the resonance at 900 MHz, but does have an influence on the depth and width of the second, wide frequency band from around 1.7 GHz to 2.7 GHz.

Next, the influence of the antenna location along the edge of the ground-plane is investigated (Fig.6). The antenna is moved along the top edge of the ground-plane. Figure 7 shows the change in the insertion loss.

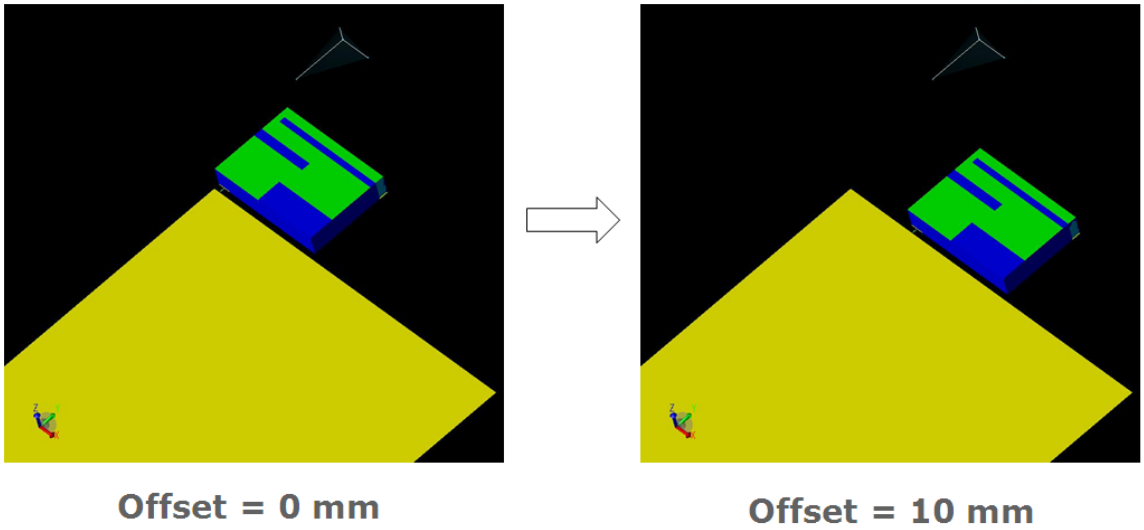


Figure 6: Definition of the off-set along the top edge of the ground plane

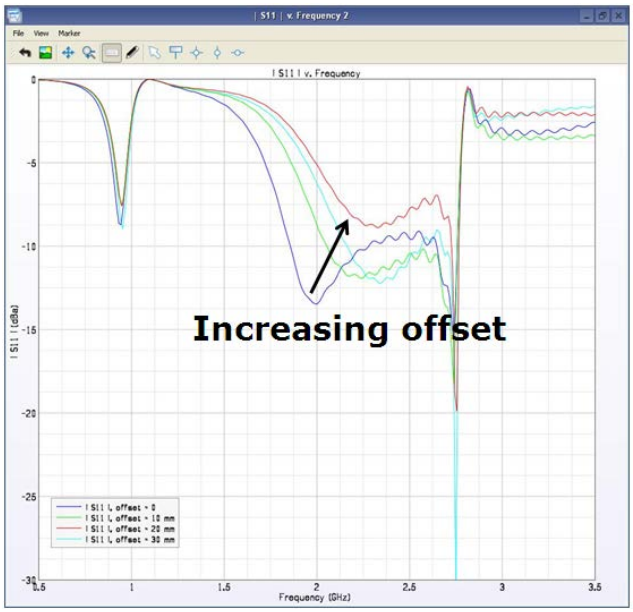


Figure 7: Influence of antenna location

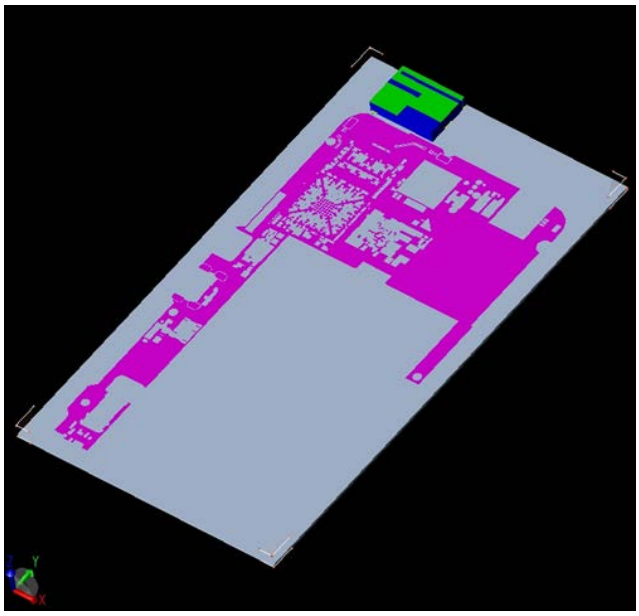
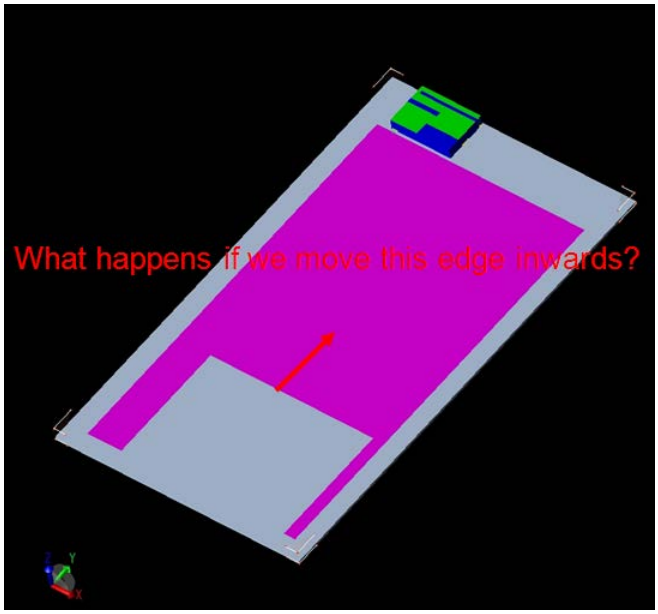


Figure 8: Real, Γ-shaped ground-plane

Figure 8 shows a real ground-plane, which looks like a Γ-shaped. The holes in this GP are voids for component placement. Figures 9 and 10 show the influence of the different large cut-outs on the antenna insertion loss when going from the simple, rectangular, solid ground-plane to a U-shaped one and then to the Γ-shaped one. It is seen that when going from a U-shaped to a Γ-shaped ground-plane, the depth of the first resonance decreases although the antenna is located at the opposite side of the leg that is being made

shorter! Figure 11 proves that even adding a vertical piece of metal to increase the length of the left leg improves the antenna performance at 900 MHz.



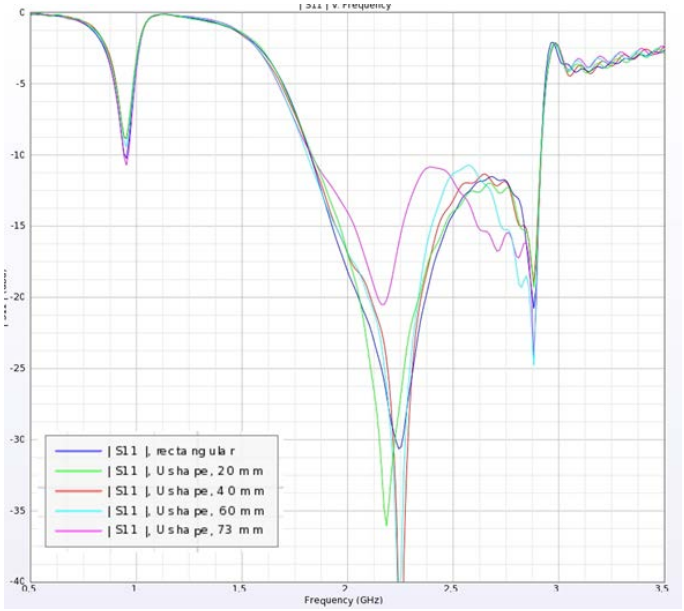
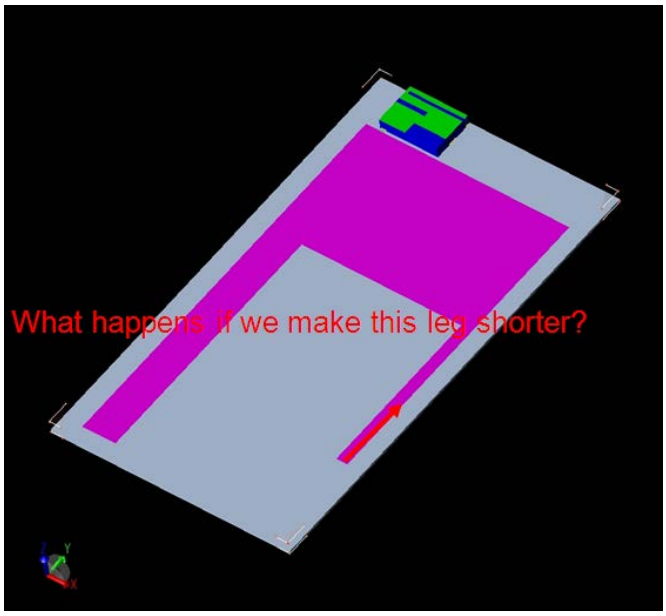


Figure 9: Influence of shape of solid ground-plane (from rectangular to U-shaped)



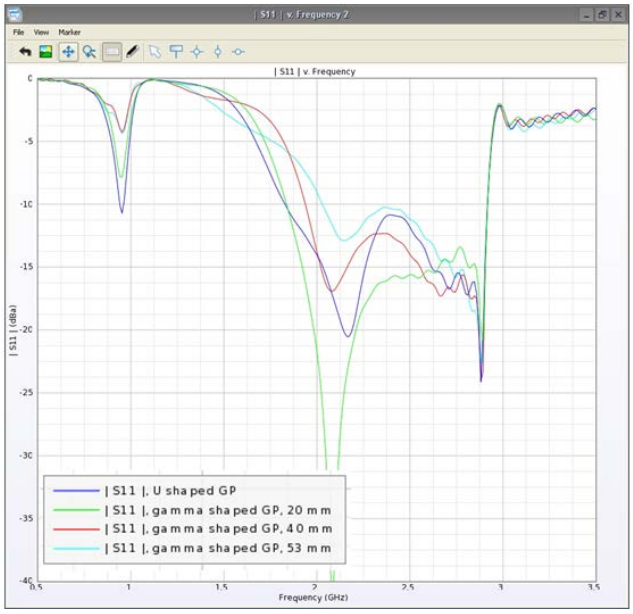


Figure 10: Influence of shape of solid ground-plane (less metal in the U-shape)

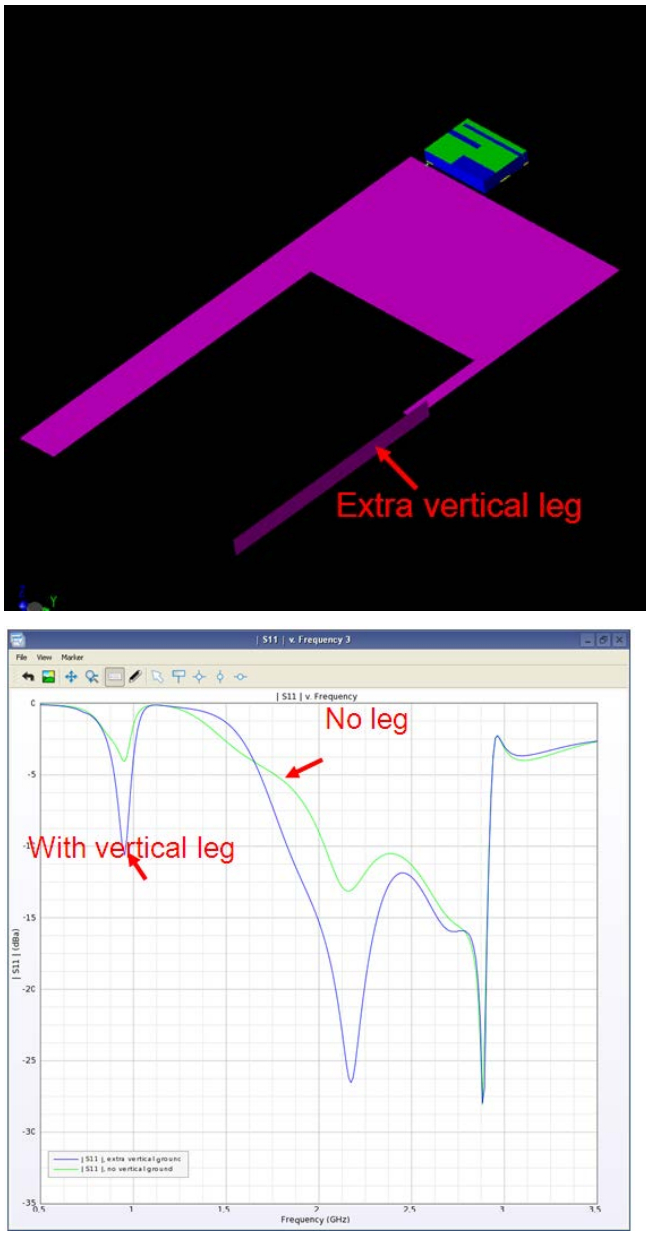


Figure 11: Influence of an extra vertical piece of metal at the right leg

These simulations already prove the importance of co-designing the on-board antenna and the PCB ground-planes. The virtual antenna/EMI lab allows looking at much more variations in a short time than can be done with physical prototypes. Moreover, the virtual antenna/EMI lab allows to look into the PCB and to determine e.g. the current distribution in the ground plane, as is shown in Figure 12 for 900 MHz and 2.4 GHz.

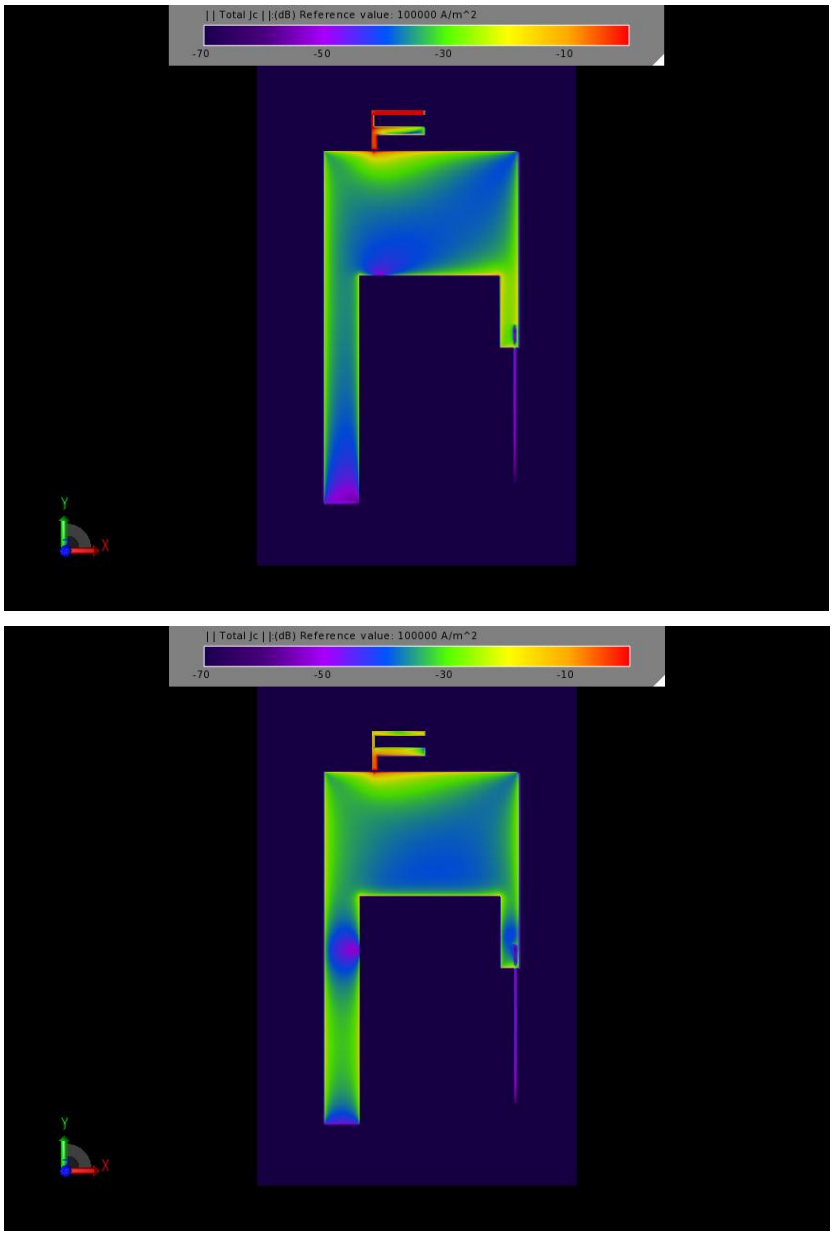


Figure 12: Surface current distribution at 900 MHz (top) and 2.4 GHz (bottom)

The current distributions also show different current signatures and hot spots at different frequencies. This aids board design in deciding where to place sensitive components on the board.

3. Crosstalk between digital and on-board antennas

3.1 PCB description

The mechanisms influencing the crosstalk between digital circuits and on-board antennas are studied based on the PCB and antenna depicted in Fig. 13.

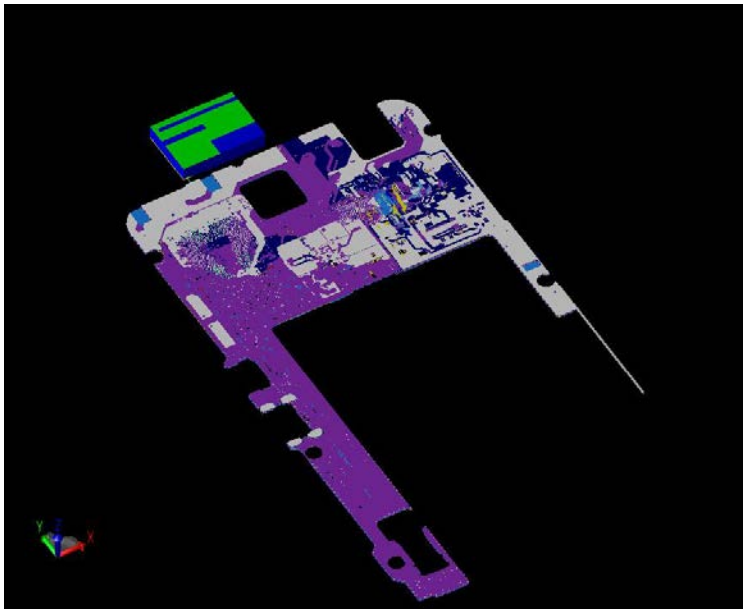


Figure 13: PCB and antenna under test

The PCB form factor was chosen for this study to be representative of a real wireless product. It has space allocated for routing three 4-bit DDR2/3 memory buses, a USB3.0 IO link and many other auxiliary circuits. The location of the antenna shown in Fig. 13 is only one of many locations on the top of the PCB to illustrate the concepts of this study. The voids shown on the PCB are spaces allocated for circuit components. The two legs on both sides are actually extensions of the ground plane to other antennas and components and the middle empty space is reserved for battery placement.

3.2 Crosstalk mechanisms

The four main coupling mechanisms that could cause the crosstalk between the traces carrying digital signals and the on-board antenna are:

1. Near-field coupling (capacitive and or inductive) “through the air” above the PCB;
2. Coupling through the excitation of waveguide modes between the different ground planes of the PCB;
3. Coupling through the overlap of the return currents of the traces and the currents induced in the ground-plane by the antenna;

4. Coupling by currents induced on the PCB by power and ground pins of active components/chips.

In the next simulations, all traces are excited in phase with 1 Volt at every port at the driver side, while the traces are loaded with 50 Ohm terminations at their other end. As the input signal is the same at all ports, a worst-case scenario is considered. The antenna port is also loaded with 50 Ohm. In order to estimate the contribution of the near-field coupling through the air and the coupling through waveguide modes between the ground planes, three cases are considered:

1. The original PCB as shown in Fig. 13;
2. The PCB with a perfect PEC shielding can above all traces on the PCB top side. This shielding can makes perfect contact with the ground plane;
3. The PCB with a perfect PEC guard ring inside the substrate and around all traces. Again this guard ring makes perfect contact with all ground planes that it intersects.

Figure 14 shows the transfer function from the input voltage of the traces to the voltage at the antenna port versus frequency for these three cases. It is seen that the applied shielding does not have a significant influence on the considered crosstalk.

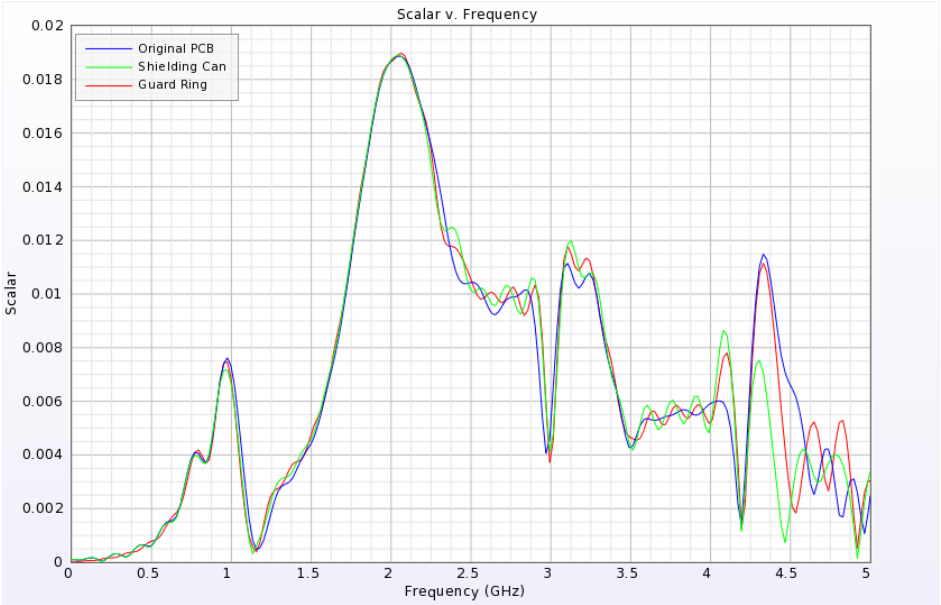


Figure 14: Transfer function from the input voltage at the traces to the voltage at the antenna port

To estimate the contribution of the coupling through the return currents and the antenna currents, two simplified structures are considered (Fig. 15). The first structure comprises the top traces above its original (real) ground plane. The second structure comprises the same traces above a solid ground plane. In the case of the solid ground-plane, there are no return path discontinuities, making the currents of the digital traces more confined to the ground plane immediately around the traces.

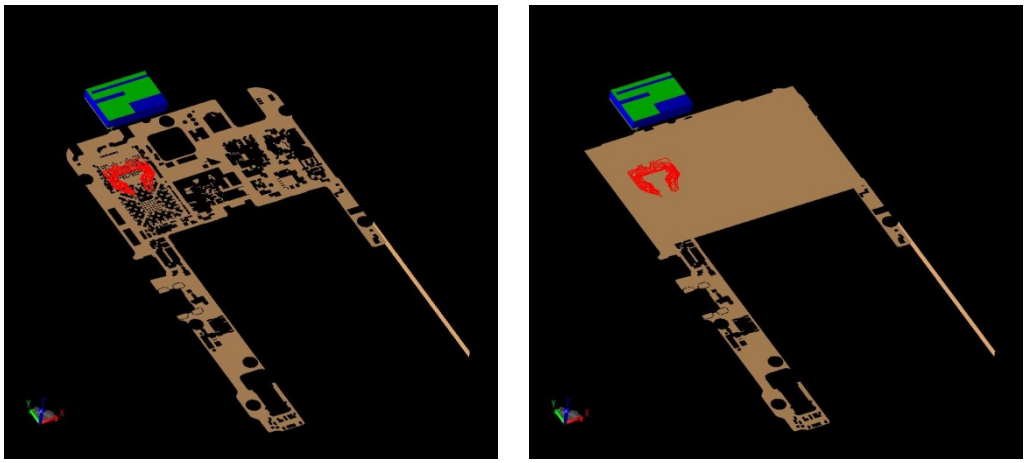


Figure 15: Top traces above original ground-plane (left) and above a solid ground-plane (right)

Figure 16 shows the time-domain noise at the antenna port when all input ports of the traces are excited with a pseudo-random bit sequence of 2GBit/s and this for the original (real) ground-plane and the solid ground-plane. The maximum amplitude in the first case is about 6.5mV while it is about 0.2mV in the second. The real GP has many discontinuities which drift the currents in other directions. These return path discontinuities have a very large influence on the noise level at the antenna port. Hence, the coupling mechanism through the overlap between the traces' and antenna's current path can be considered as the main contributing factor of noise. . Hence, during the placement stage of components on the PCB one has to carefully select the place where one will put the digital interfaces, keeping in mind the antenna current profiles. Moreover, one has to avoid any current return path discontinuities to prevent large current coupling.

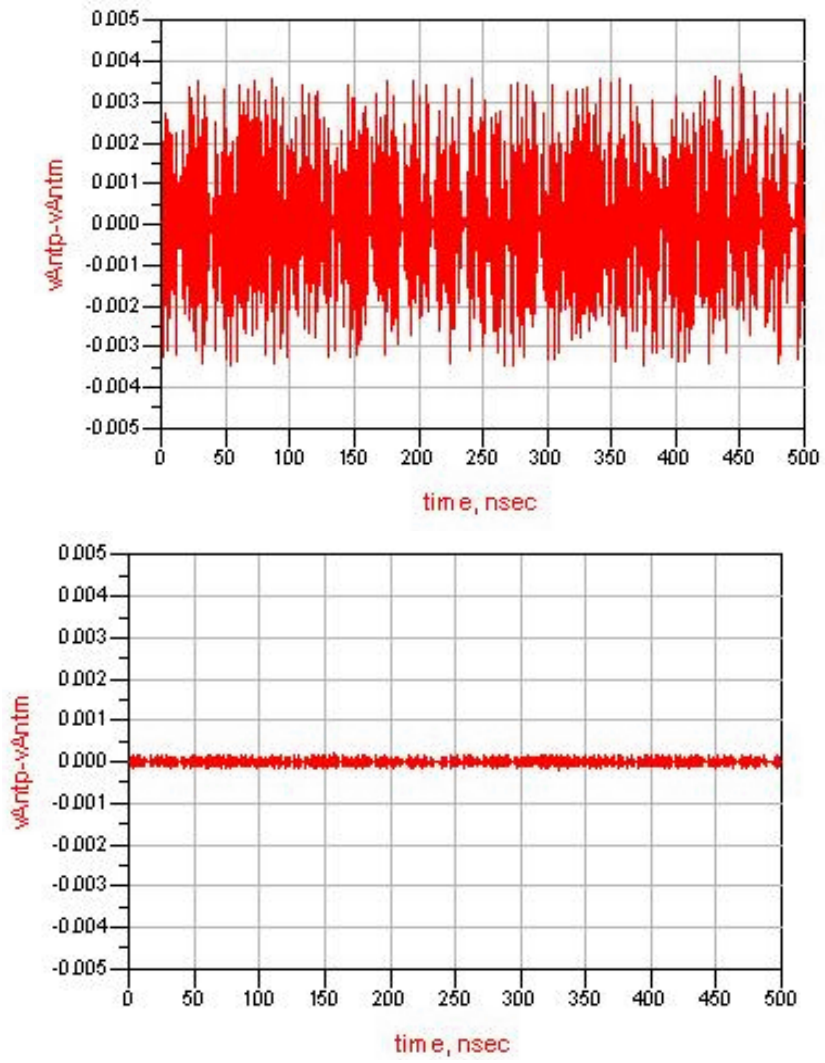


Figure 16: Time domain noise voltage (in mV) at the antenna port for the original (real) ground-plane (top) and the solid ground-plane (bottom).

4. Noise mitigation through phase-shifting

One way to reduce the coupling from the digital interfaces to the on-board antennas without affecting the routing of an existing PCB layout is to intentionally apply a phase shift (time delay) between the different input ports. To investigate this, the input ports on the original PCB shown in Fig. 13 are divided into four groups:

- Group#1: The input ports connecting to the traces at the top layer and at the left side;
- Group#2: The input ports connecting to the traces at the top layer and at the right side;
- Group#3: The input ports connecting to the traces at the bottom layer and at the left side;

- Group#4: The input ports connecting to the traces at the bottom layer and at the right side.

A phase shift is applied by giving each group a specified time delay. Group#1 is the reference group and has no time delay, group#2 has a time delay Δ, group#3 a time delay 2Δ, and group#4 a time delay 3Δ. Figure 17 shows the frequency transfer function from the input voltage to voltage at the antenna port for Δ equal to 235ps. It is seen that for a time delay of Δ and 3Δ, the coupling is significantly reduced (by about 50%) up to 2.5 GHz.

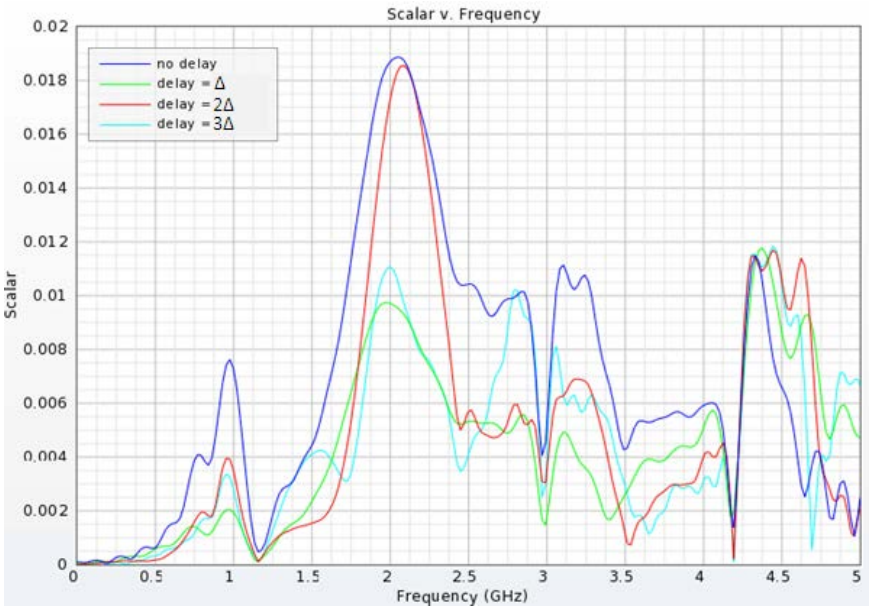


Figure 17: Transfer function from the input voltage at the traces to the voltage at the antenna port for different delay between the input groups.

5. Conclusion

In this paper, it was shown that the coupling between digital interfaces is an important aspect for the overall performance of a PCB with on-board antenna modules. The crosstalk is a two-way problem. In receive mode, the crosstalk from the digital interface to the antenna reduces the sensitivity of the receiving module. In transmit mode, the crosstalk from the antenna to the digital interfaces deteriorates the eye diagram and might lead to higher bit error rates. It was shown that the interaction between the return currents of the digital interfaces and the antenna current profiles in the ground-planes is the main contributor to the crosstalk. During the design, the antenna current distribution has to be taken into account when deciding on the location of the digital interfaces. Current path discontinuities have to be avoided. Finally, applying an appropriate time-delay between the different byte lanes can reduce the crosstalk from the digital interfaces onto the on-board antennas by about 50%.

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